

What is claimed is:

1. A phase-locked loop circuit comprising:

a phase comparison means for detecting a size
of a leading phase or a delayed phase of a feedback
5 signal with respect to a reference signal and outputting
a leading phase signal having a pulse width corresponding
to the size of the leading phase or a delayed phase
signal having a pulse width corresponding to the size of
the delayed phase;

10 a smoothing means for smoothing the leading
phase signal or the delayed phase signal output from the
phase comparison means and outputting the result as a
control signal;

a superposing means for superposing the leading
15 phase signal or the delayed phase signal output from the
phase comparison means on the control signal; and

an oscillation circuit for receiving the
control signal superposed with other signals by the
superposing means and outputting the feedback signal of a
20 frequency corresponding to the control signal to the
phase comparison means.

2. A phase-locked loop circuit as set forth in
claim 1, wherein the superposing means includes a
capacitor receiving the leading phase signal or the
25 delayed phase signal at one terminal and connected to an

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output line of the control signal of the smoothing means at another terminal.

3. A phase-locked loop circuit as set forth in claim 2, wherein

5 the smoothing means includes

a current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal and

10 a filter for outputting said control signal obtained by smoothing the output current from the current outputting means.

4. A phase-locked loop circuit as set forth in claim 2, wherein

15 the smoothing means includes

a current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal,

20 a series circuit having a resistor and a capacitor receiving the output current from the current outputting means, and

a noise filter for receiving the voltage of the series circuit and outputting said control signal after removing noise components included in the voltage.

25 5. A phase-locked loop circuit as set forth in claim 4, wherein

the current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

6. A phase-locked loop circuit as set forth in
5 claim 2, wherein

the smoothing means includes

a first current outputting means and a second current outputting means for outputting a current corresponding to the leading phase signal or a current
10 corresponding to the delayed phase signal,

a series circuit having a resistor receiving the output current from the first current outputting means and a capacitor receiving a current of the resistor and the output current from the second current outputting
15 means, and

a noise filter for receiving the voltage of the series circuit and outputting said control signal after removing noise components included in the voltage.

7. A phase-locked loop circuit as set forth in
20 claim 6, wherein

the first current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

8. A phase-locked loop circuit as set forth in
25 claim 6, wherein

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the second current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

9. A phase-locked loop circuit as set forth in
5 claim 1, wherein

the phase comparison means activates or deactivates outputs of the leading phase signal and the delayed phase signal to the superposing means according to a mode selecting signal.

10 10. A phase-locked loop circuit as set forth in claim 1, wherein

the phase comparison means adjusts pulse amplitudes of the leading phase signal and the delayed phase signal according to a pulse amplitude adjusting
15 signal.

11. A phase-locked loop circuit as set forth in claim 1, wherein

the phase comparison means selects at least one leading phase signal or delayed phase signal from a
20 plurality of the leading phase signals or the delayed phase signals according to a pulse amplitude adjusting signal and outputs it to the superposing means, and

the superposing means includes at least one capacitor receiving the leading phase signal or the
25 delayed phase signal at one terminal and connected to an

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output line of the control signal of the smoothing means at another terminal.

12. A phase-locked loop circuit as set forth in claim 1, wherein

5 the phase comparison means adjusts pulse widths of the leading phase signal and the delayed phase signal according to a pulse width adjusting signal.

13. A phase-locked loop circuit comprising
 a phase comparison means for detecting a size
10 of a leading phase or a delayed phase of a feedback signal with respect to a reference signal and outputting a leading phase signal having a pulse width corresponding to the size of the leading phase or a delayed phase
15 signal having a pulse width corresponding to the size of the delayed phase,

 a smoothing means for smoothing the leading phase signal or the delayed phase signal output from the phase comparison means and outputting the result as a control signal,

20 a bias signal generating means for outputting a first bias signal and a second signal corresponding to the control signal,

 a noise filter for removing noise components included in the first bias signal and the second signal,

25 a first superposing means for superposing the

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leading phase signal or the delayed phase signal output
from the phase comparison means on the first bias signal,

a second superposing means for superposing the
leading phase signal or the delayed phase signal output

5 from the phase comparison means on the second bias
signal, and

an oscillation circuit which includes a
plurality of delay stages for exchanging and outputting a
first current variable according to the first bias signal

10 superposed with other signals by the first superposing
means and a second current variable according to the
second bias signal superposed with other signals by the
second superposing means according to levels of input
signals, feeds back an output signal of a last delay
15 stage to an input of a first delay stage, and outputs an
output signal of one of the delay stages as the feedback
signal to the phase comparison means.

14. A phase-locked loop circuit as set forth in
claim 13, wherein

20 the first superposing means includes a
capacitor receiving the leading phase signal or the
delayed phase signal at one terminal and connected to an
output line of the first bias signal of the bias signal
generating means at another terminal, and

25 the second superposing means includes a

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capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the second bias signal of the bias signal generating means at another terminal.

5 15. A phase-locked loop circuit as set forth in claim 13, wherein

the smoothing means includes

a current outputting means for outputting a current corresponding to the leading phase signal or a
10 current corresponding to the delayed phase signal and

a series circuit having a resistor and a capacitor receiving the output current from the current outputting means, and

the bias signal generating means generates the
15 first bias signal and the second bias signal according to a voltage of the series circuit.

16. A phase-locked loop circuit as set forth in claim 15, wherein

the current outputting means adjusts an
20 amplitude of the output current according to a current adjusting signal.

17. A phase-locked loop circuit as set forth in claim 13, wherein

the smoothing means includes

25 a first current outputting means and a second

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current outputting means for outputting a current
corresponding to the leading phase signal or a current
corresponding to the delayed phase signal and

a series circuit having a resistor receiving
5 the output current from the first current outputting
means and a capacitor receiving a current of the resistor
and the output current from the second current outputting
means, and

the bias signal generating means generates the
10 first bias signal and the second bias signal according to
a voltage of the series circuit.

18. A phase-locked loop circuit as set forth in
claim 17, wherein the first current outputting means
adjusts an amplitude of the output current according to a
15 current adjusting signal.

19. A phase-locked loop circuit as set forth in
claim 17, wherein the second current outputting means
adjusts an amplitude of the output current according to a
current adjusting signal.

20 20. A phase-locked loop circuit as set forth in
claim 13, wherein the phase comparison means activates or
deactivates outputs of the leading phase signal and the
delayed phase signal to the superposing means according
to a mode selection signal.

25 21. A phase-locked loop circuit as set forth in

claim 13, wherein the phase comparison means adjusts amplitudes of the leading phase signal and the delayed phase signal according to a pulse amplitude adjusting signal.

5 22. A phase-locked loop circuit as set forth in claim 13, wherein

 the phase comparison means selects at least one leading phase signal or delayed phase signal from a plurality of the leading phase signals or the delayed
10 phase signals according to a pulse amplitude adjusting signal and outputs it to the first superposing means and the second superposing means,

 the first superposing means includes at least one capacitor receiving the leading phase signal or the
15 delayed phase signal at one terminal and connected to an output line of the first bias signal of the bias signal generating means at another terminal, and

 the second superposing means includes at least one capacitor receiving the leading phase signal or the
20 delayed phase signal at one terminal and connected to an output line of the second bias signal of the bias signal generating means at another terminal.

 23. A phase-locked loop circuit as set forth in claim 13, wherein the phase comparison means adjusts
25 pulse widths of the leading phase signal and the delayed

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phase signal according to a pulse width adjusting signal.

24. A delay-locked loop circuit comprising

a phase comparison means for detecting a size
of a leading phase or a delayed phase of a feedback
5 signal with respect to a reference signal and outputting
a leading phase signal having a pulse width corresponding
to the size of the leading phase or a delayed phase
signal having a pulse width corresponding to the size of
the delayed phase,

10 a smoothing means for smoothing the leading
phase signal or the delayed phase signal output from the
phase comparison means and outputting the result as a
control signal,

a superposing means for superposing the leading
15 phase signal or the delayed phase signal output from the
phase comparison means on the control signal, and

a delay circuit for receiving the control
signal superposed with other signals by the superposing
means and the reference signal and outputting to the
20 phase comparison means the feedback signal having a delay
corresponding to the control signal relative to the
reference signal.

25. A delay-locked loop circuit as set forth in
claim 24, wherein

25 the superposing means includes a capacitor

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receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the control signal of the smoothing means at another terminal.

5 26. A delay-locked loop circuit as set forth in claim 25, wherein

the smoothing means includes

 a current outputting means for outputting a current corresponding to the leading phase signal or a
10 current corresponding to the delayed phase signal and
 a filter for outputting a control signal obtained by smoothing the output current from the current outputting means.

 27. A delay-locked loop circuit as set forth in
15 claim 25, wherein

the smoothing means includes

 a current outputting means for outputting a current corresponding to the leading phase signal or a current corresponding to the delayed phase signal,
20 a series circuit having a resistor and a capacitor receiving the output current from the current outputting means, and

 a noise filter for receiving the voltage of the series circuit and outputting said control signal after
25 removing noise components included in the voltage.

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28. A delay-locked loop circuit as set forth in claim 27, wherein the current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

5 29. A delay-locked loop circuit as set forth in claim 25, wherein

the smoothing means includes

a first current outputting means and a second current outputting means for outputting a current
10 corresponding to the leading phase signal or a current corresponding to the delayed phase signal,

a series circuit having a resistor receiving the output current from the first current outputting means and a capacitor receiving a current of the resistor
15 and the output current from the second current outputting means, and

a noise filter for receiving the voltage of the series circuit and outputting said control signal after removing noise components included in the voltage.

20 30. A delay-locked loop circuit as set forth in claim 29, wherein

the first current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

25 31. A delay-locked loop circuit as set forth in

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claim 29, wherein

the second current outputting means adjusts an amplitude of the output current according to a current adjusting signal.

5 32. A delay-locked loop circuit as set forth in claim 24, wherein

the phase comparison means activates or deactivates outputs of the leading phase signal and the delayed phase signal to the superposing means according
10 to a mode selection signal.

33. A delay-locked loop circuit as set forth in claim 24, wherein

the phase comparison means adjusts pulse amplitudes of the leading phase signal and the delayed
15 phase signal according to a pulse amplitude adjusting signal.

34. A delay-locked loop circuit as set forth in claim 24, wherein

the phase comparison means selects at least one
20 leading phase signal or delayed phase signal from a plurality of the leading phase signals or the delayed phase signals according to a pulse amplitude adjusting signal and outputs it to the superposing means, and

the superposing means includes at least one
25 capacitor receiving the leading phase signal or the

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delayed phase signal at one terminal and connected to an output line of the control signal of the smoothing means at another terminal.

35. A delay-locked loop circuit as set forth in
5 claim 24, wherein

the phase comparison means adjusts pulse widths of the leading phase signal and the delayed phase signal according to a pulse width adjusting signal.

36. A delay-locked loop circuit comprising
10 a phase comparison means for detecting a size of a leading phase or a delayed phase of a feedback signal with respect to a reference signal and outputting a leading phase signal having a pulse width corresponding to the size of the leading phase or a delayed phase
15 signal having a pulse width corresponding to the size of the delayed phase,

a smoothing means for smoothing the leading phase signal or the delayed phase signal output from the phase comparison means and outputting the result as a
20 control signal,

a bias signal generating means for outputting a first bias signal and a second bias signal corresponding to the control signal,

a noise filter for removing noise components
25 included in the first bias signal and the second signal,

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a first superposing means for superposing the leading phase signal or the delayed phase signal output from the phase comparison means on the first bias signal,

a second superposing means for superposing the leading phase signal or the delayed phase signal output from the phase comparison means on the second bias signal, and

a delay circuit which includes a plurality of delay stages for exchanging and outputting a first current variable according to the first bias signal superposed with other signals by the first superposing means and a second current variable according to the second bias signal superposed with other signals by the second superposing means according to levels of input signals, inputs the reference signal to a first delay, and outputs an output signal of one of the delay stages as the feedback signal to the phase comparison means.

37. A delay-locked loop circuit as set forth in claim 36, wherein

the first superposing means includes a capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the first bias signal of the bias signal generating means at another terminal, and

the second superposing means includes a

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capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an output line of the second bias signal of the bias signal generating means at another terminal.

5 38. A delay-locked loop circuit as set forth in claim 36, wherein

the smoothing means includes

a current outputting means for outputting a current corresponding to the leading phase signal or a
10 current corresponding to the delayed phase signal, and

a series circuit having a resistor and a capacitor receiving the output current from the current outputting means, and

the bias signal generating means generates the
15 first bias signal and the second bias signal according to a voltage of the series circuit.

39. A delay-locked loop circuit as set forth in claim 38, wherein the current outputting means adjusts an amplitude of the output current according to a current
20 adjusting signal.

40. A delay-locked loop circuit as set forth in claim 36, wherein

the smoothing means includes

a first current outputting means and a second
25 current outputting means for outputting a current

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corresponding to the leading phase signal or a current
corresponding to the delayed phase signal and

a series circuit having a resistor receiving
the output current from the first current outputting
5 means and a capacitor receiving a current of the resistor
and the output current from the second current outputting
means, and

the bias signal generating means generates the
first bias signal and the second bias signal according to
10 a voltage of the series circuit.

41. A delay-locked loop circuit as set forth in
claim 40, wherein the first current outputting means
adjusts an amplitude of the output current according to a
current adjusting signal.

15 42. A delay-locked loop circuit as set forth in
claim 40, wherein the second current outputting means
adjusts an amplitude of the output current according to a
current adjusting signal.

43. A delay-locked loop circuit as set forth in
20 claim 36, wherein the phase comparison means activates or
deactivates outputs of the leading phase signal and the
delayed phase signal to the superposing means according
to a mode selection signal.

44. A delay-locked loop circuit as set forth in
25 claim 36, wherein the phase comparison means adjusts

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amplitudes of the leading phase signal and the delayed phase signal according to a pulse amplitude adjusting signal.

45. A delay-locked loop circuit as set forth in
5 claim 36, wherein

the phase comparison means selects at least one leading phase signal or delayed phase signal from a plurality of the leading phase signals or the delayed phase signals according to a pulse amplitude adjusting
10 signal and outputs it to the first superposing means and the second superposing means,

the first superposing means includes at least one capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an
15 output line of the first bias signal of the bias signal generating means at another terminal, and

the second superposing means includes at least one capacitor receiving the leading phase signal or the delayed phase signal at one terminal and connected to an
20 output line of the second bias signal of the bias signal generating means at another terminal.

46. A delay-locked loop circuit as set forth in claim 36, wherein the phase comparison means adjusts pulse widths of the leading phase signal and the delayed
25 phase signal according to a pulse width adjusting signal.

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